Introduction to Digital Logic Design Lab

EECS 31L

Lab 5: RISC-V Single Cycle Processor.

3/1/2020

1, Objective

In this lab, I intended to design a RISC-V Single Cycle Processor.

2, Procedure

The RISC-V Single Cycle Processor is a very complex system that contains several submodules. The design of the processor can be divided to the design of submodules and the combination of submodules, which are complicated compared to the design of a single module. The processor has several submodules such as Regfile, FlipFlop, Half\_adder, Instr\_mem, ImmGen, Alu, Data\_mem and two Mux. Regfile, FlipFlop and Instr\_mem were designed in the pervious lab.

For Half\_adder, I used 2 inputs and one output, and one of the inputs is fixed to 4 because it adds pc with 4 each time.

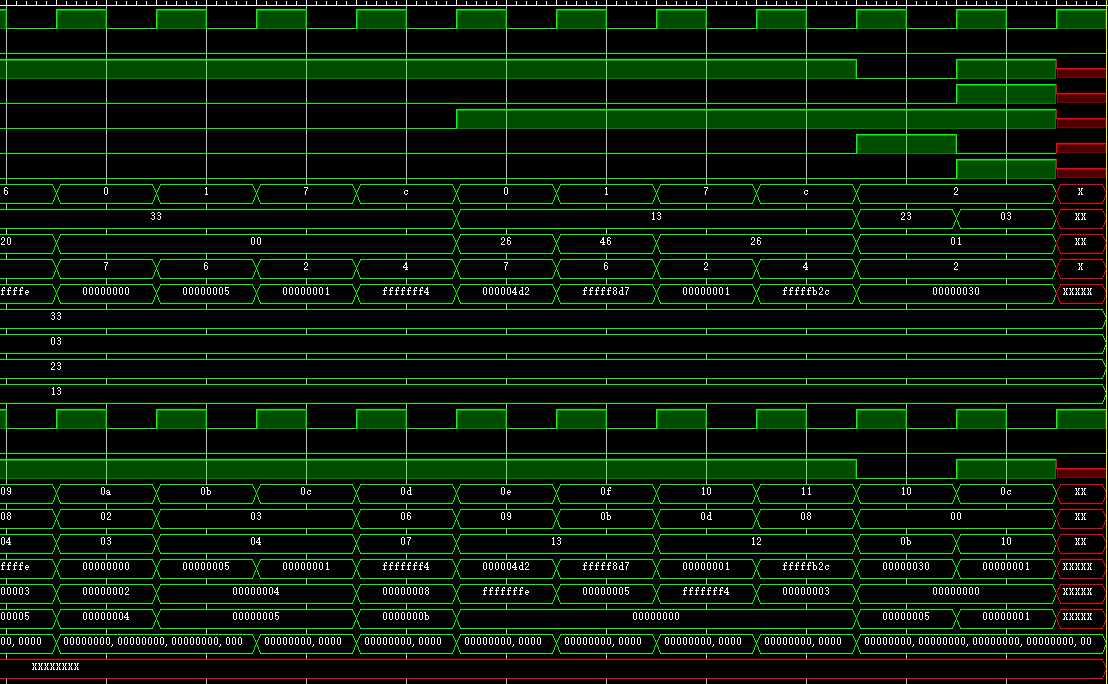
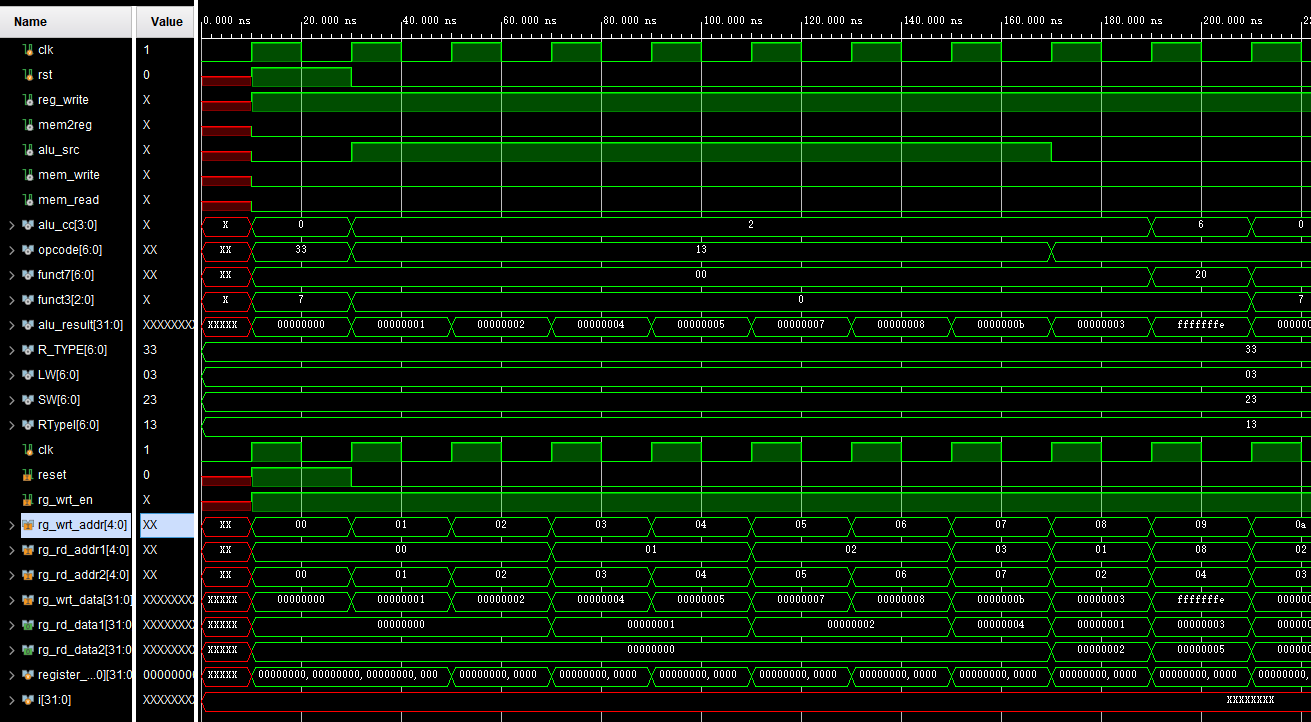
For Imm\_Gen and alu, professor already provided code.

For those two 2 to 1 Mux, the two inputs are 32 bits, and the output is 32 bits.

For data\_mem, the design is bit similar to the design of Regfile, I created a 2-dimensional array, which is 128 \* 32.

However, what I was frustrated was that I didn’t get the [i] variable under RegFile right

3, Simulation Results



Under is the whole pic…….(too big so I separated it into 2)

